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Carry Select Adder Circuit with A Successively Incremented Carry Number Block

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ABSTRACT
This paper reports a conditional carry select (CCS) adder circuit with a successively-incremented-carry-number block (SICNB) structure for low-voltage VLSI implementation. Owing to the successively-incremented-carry-number block (SICNB) structure, the new 16-bit SICNB CCS adder provides a 37% faster speed as compared to the conventional conditional Carry select adder based on the SPICE results.

***Keywords* -** Carry Select Adder, SICNB Carry Select Adder, PTBCS Circuit.

I. INTRODUCTION

Addition usually impacts widely the overall performance of digital systems and a crucial arithmetic function. In electronic applications adders are most widely used. Applications where these are used are multipliers, DSP to execute various algorithms like FFT, FIR and IIR. Wherever concept of multiplication comes adders come in to the picture. As we know millions of instructions per second are performed in microprocessors. So, speed of operation is the most important constraint to be considered while designing multipliers. Due to device portability miniaturization of device should be high and power consumption should be low. Devices like Mobile, Laptops etc. require more battery backup. So, a VLSI designer has to optimize these three parameters in a design. These constraints are very difficult to achieve so depending on demand or application some compromise between constraints has to be made. Ripple carry adders exhibits the most compact design but the slowest in speed. Whereas carry lookahead is the fastest one but consumes more area . Carry select adders act as a compromise between the two adders. The speed performance of a CPU is predominantly determined by its adder circuit. Various adder circuits with improved speed performance have been reported. Among them, the conditional carry select (CCS) adder has a superior speed performance in a 16-bit CCS adder, the key circuit is the carry select circuit.

II. OPERATION

The principle of the carry select circuit is briefly described here. The carry select circuit is used to process the propagate and generate signals produced by the half adders to generate the carry signals. The function of the carry select circuit is-

C(i)=G(i)+C(i-1).P(i) For i=1~n
G(i)=X(i).Y(i)
P(i)=X(i)+Y(i)

$$C_i = \overline{C_{i-1}} \cdot G_i + C_{i-1} \cdot P_i.$$

the 16-bit conditional carry select circuit is group into four carry blocks. In each carry block, there are four multiplexers (MUX) controlled by C(i-1) to produce four output carry signals C(i), C(i-1), C(i-2),C(i-3) the carry number of this conditional carry select circuit is four

$$C_i = \overline{C_j} \cdot C_i(\text{if } C_j = 0) + C_j \cdot C_i(\text{if } C_j = 1)$$
$$i = j+1 \sim j+4;\ j = -1, 3, 7, 11.$$

For example, in the first block, considering Co, if Cin=1, the output carry signal

$$\text{If } C_{\text{in}} = 0$$

$$\begin{aligned} C_3 = {} & \overline{\overline{\overline{G_0} \cdot G_1 + G_0 \cdot P_1} \cdot G_2 + (\overline{G_0} \cdot G_1 + G_0 \cdot P_1) \cdot P_2} \cdot G_3 \\ & + (\overline{\overline{G_0} \cdot G_1 + G_0 \cdot P_1} \cdot G_2 \\ & + (\overline{G_0} \cdot G_1 + G_0 \cdot P_1) \cdot P_2) \cdot P_3 \\ \equiv {} & C_3(\text{if } C_{\text{in}} = 0). \end{aligned}$$

$$C_0 = \overline{C_{in}} \cdot G_o + C_{in} \cdot P_0 = P_0 \equiv C_0(\text{if } C_{in} = 1).$$

If

$$C_{in} = 0, \quad C_0 = G_0 \equiv C_0(\text{if } C_{in} = 0).$$

As for C_1, if $C_{in} = 1$

$$\begin{aligned} C_1 &= \overline{C_0} \cdot G_1 + C_0 \cdot P_1 \\ &= \overline{P_0} \cdot G_1 + P_0 \cdot P_1 \equiv C_1(\text{if } C_{in} = 1). \end{aligned}$$

If $C_{in} = 0$

$$C_1 = \overline{G_0} \cdot G_1 + G_o \cdot P_1 \equiv C_1(\text{if } C_{in} = 0).$$

As for C_2, if $C_{in} = 1$

$$\begin{aligned} C_2 &= \overline{C_1} \cdot G_2 + C_1 \cdot P_2 \\ &= \overline{\overline{P_0} \cdot G_1 + P_0 \cdot P_1} \cdot G_2 + (\overline{P_0} \cdot G_1 + P_0 \cdot P_1) \cdot P_2 \\ &\equiv C_2(\text{if } C_{in} = 1). \end{aligned}$$

If $C_{in} = 0$

$$\begin{aligned} C_2 &= \overline{\overline{G_0} \cdot G_1 + G_0 \cdot P_1} \cdot G_2 + (\overline{G_0} \cdot G_1 + G_0 \cdot P_1) \cdot P_2 \\ &\equiv C_2(\text{if } C_{in} = 0). \end{aligned}$$

As for C_3, if $C_{in} = 1,$

$$\begin{aligned} C_3 &= \overline{C_2} \cdot G_3 + C_2 \cdot P_3 \\ &= \overline{\overline{\overline{P_0} \cdot G_1 + P_0 \cdot P_1} \cdot G_2 + (\overline{P_0} \cdot G_1 + P_0 \cdot P_1) \cdot P_2} \cdot G_3 \\ &\quad + (\overline{\overline{P_0} \cdot G_1 + P_0 \cdot P_1} \cdot G_2 \\ &\quad + (\overline{P_0} \cdot G_1 + P_0 \cdot P_1) \cdot P_2) \cdot P_3 \\ &\equiv C_3(\text{if } C_{in} = 1). \end{aligned}$$

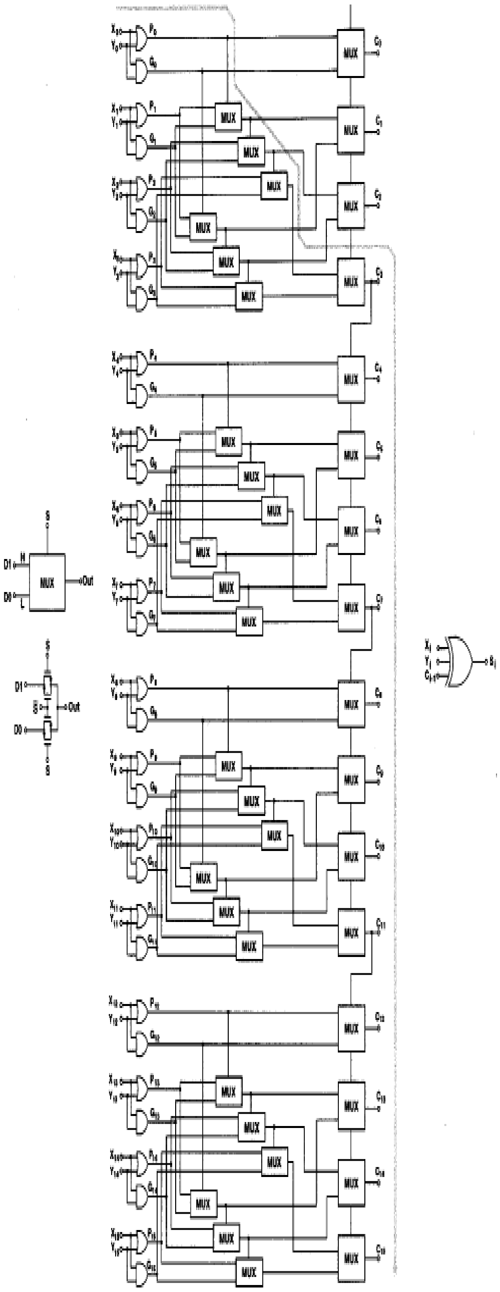

Fig.1.Block diagram of a 16-bit CCS circuit.

In summary, there are four carry blocks in the 16-bit conditional carry select circuit. Each carry block produces four output carry signals. In the first block, with the multiplexer control signalCin , four output carry signals (Co,C1,C2,C3) are produced. In the second block, with the multiplexer control signal C3, four output carry signals (C4, C5, C6, C7) are generated. In the third block, with the multiplexer control signal C7, four output carry signals (C8 ,C9 ,C10 ,C11) are produced. With the multiplexer control signalC11, four output carry signals (C12,C13,C14,C15) are generated. The longest critical path is From Xo to C15 , which occurs at inputs (Xo~X15)=(1,0~0); (Yo~Y15) =(1~1) , which involves gate delays of eight stages—one stage of Po or Go , three stages of multiplexers, and four stages of carry.

III. CARRY SELECT ADDER (CSA)

The carry select adder comes in the category of conditional sum adder.Conditional sum adder works on some condition. Sum and carry are calculated by assuming input carry as 1 and 0 prior theinput carry comes. When actual carry input arrives, the actual calculated values of sum and carry are selected using a multiplexer. The conventional carry select adder consists of k/2 bit adder for the lower half of the bits i.e. least significant bits and for the upper half i.e. most significant bits (MSB's) two k/ bit adders. In MSB adders one adder assumes carry input as one for performing addition and another assumes carry input as zero.The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of output carry and sum. The selection is done by using a multiplexer. This technique of dividing adder in to stages increases the area utilization but addition operation fastens. The carry-select adder is one of the faster types of adders, and has smaller area overhead than all other types of adders except for the carry-skip adder. The main difference between a carry-select adder and a ripple-carry adder is that in a ripple-carry adder the carry has to ripple through all full-adders, but in the case of a carry-select adder the carry has to pass through a single multiplexer. As discussed above, the carry-select addition process results in faster addition. To guarantee reliable operation of such an adder the detection of faults in the adder, especially transient faults, is extremely important. The probability of transient faults occurring in modern VLSI systems has grown significantly because of the shrinkage in transistor dimensions.

IV. SUCCESSIVELY INCREMENTED CARRY NUMBER BLOCK (SICNB) CARRY SELECT ADDER

The 16-bit SICNB CCS circuit. As shown in the figure, five carry blocks, as in the conditional carry select circuit, have been used. Different from the conditional carry select circuit, the carry number in each carry block is not always four—not uniform. Instead, in the first carry block, only one output carry signal Co is produced

$$C_i = \overline{C_j} \cdot C_i(\text{if } C_j = 0) + C_j \cdot C_i(\text{if } C_j = 1);$$
$$j = -1, i = j + 1.$$

In the second carry block, two output carry signals C1 and C2 are generated.

$$C_i = \overline{C_j} \cdot C_i(\text{if } C_j = 0) + C_j \cdot C_i(\text{if } C_j = 1);$$
$$j = -1, i = j + 1.$$

In the third carry block, three output carry signals C3 –C5 are available

$$C_i = \overline{C_j} \cdot C_i(\text{if } C_j = 0) + C_j \cdot C_i(\text{if } C_j = 1);$$
$$j = 2, i = j + 1 \sim j + 3.$$

In the fourth carry block, four output carry signalsC6 –C9 are generated.

$$C_i = \overline{C_j} \cdot C_i(\text{if } C_j = 0) + C_j \cdot C_i(\text{if } C_j = 1);$$
$$j = 5, i = j + 1 \sim j + 4.$$

In the fifth carry block, six output carry signalsC10 –C15 are produced

$$C_i = \overline{C_j} \cdot C_i(\text{if } C_j = 0) + C_j \cdot C_i(\text{if } C_j = 1);$$
$$j = 9, i = j + 1 \sim j + 6.$$

As shown in the figure, in the SICNB CCS adder, the number of output carry signals produced in each block is successively incremented from the first block to the last block.

The longest critical path is from Xo to X15, which occurs at inputs (Xo~X15)=(1,0~0);(Yo~Y15)=(1~1) , which involves gate delays of six stages one stage of or and five stages of multiplexers. Compared to the conventional conditional carry select circuit, the longest critical path is two stages shorter.

Fig. 3 shows the 1-bit pass-transistor-based carry select (PTBCS) circuit used in the SICNB CCS adder of Fig. Instead Pi of in the conventional Manchester CLA circuit, Ci-1 is used as the control signal in the PTBCS circuit, as shown in Fig. 3. In addition, pass-transistor logic has been used to replace the multiplexer structure. The operation principle is described here. When Ci-1 , the carry signal (Ci=Gi+ci-1.Pi) becomesCi=Pi , hence is used as the input to a transmission gate controlled byCi-1 . When Ci-1=0, the transmission gate is off. Under this situation, the circuit is similar to aGi -controlled inverter (when Ci-1is high; hence, the NMOS device MNA is on). Therefore, Ci=Gi. Similarly

$$\overline{C_i} = \overline{G_i}\cdot\left(\overline{C_{i-1}}+\overline{P_i}\right) = \overline{C_{i-1}}\cdot\overline{G_i}+\overline{G_i}\cdot\overline{P_i}.$$

Since

$$\overline{G_i}\cdot\overline{P_i} = \left(\overline{X_i}+\overline{Y_i}\right)\left(\overline{X_i}\cdot\overline{Y_i}\right) = \overline{X_i}\cdot\overline{Y_i} = \overline{P_i}$$

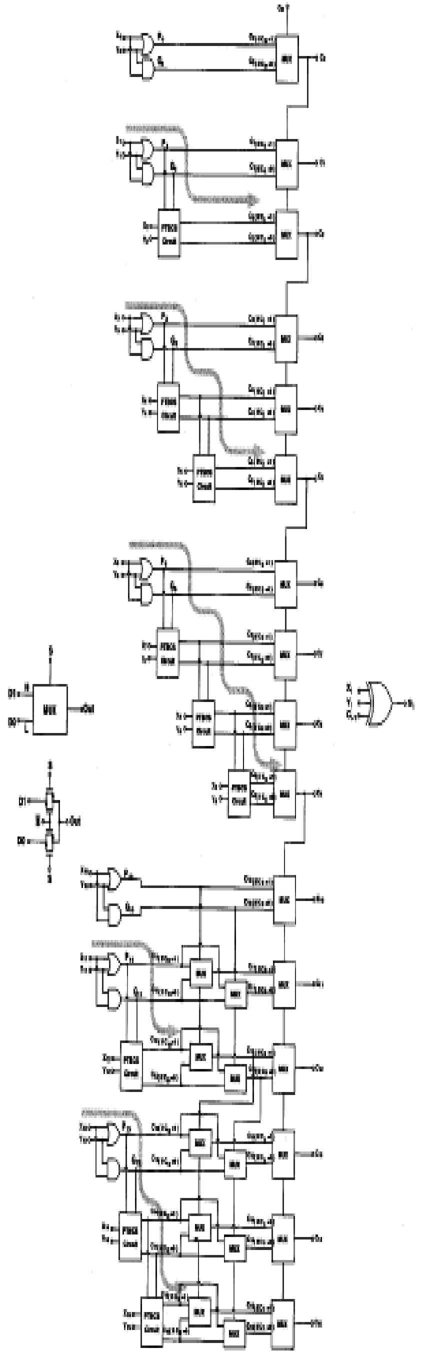

Fig.2 Block diagram of the 16-bit SICNB structure CCS circuit.

V. PTBCS CIRCUIT:

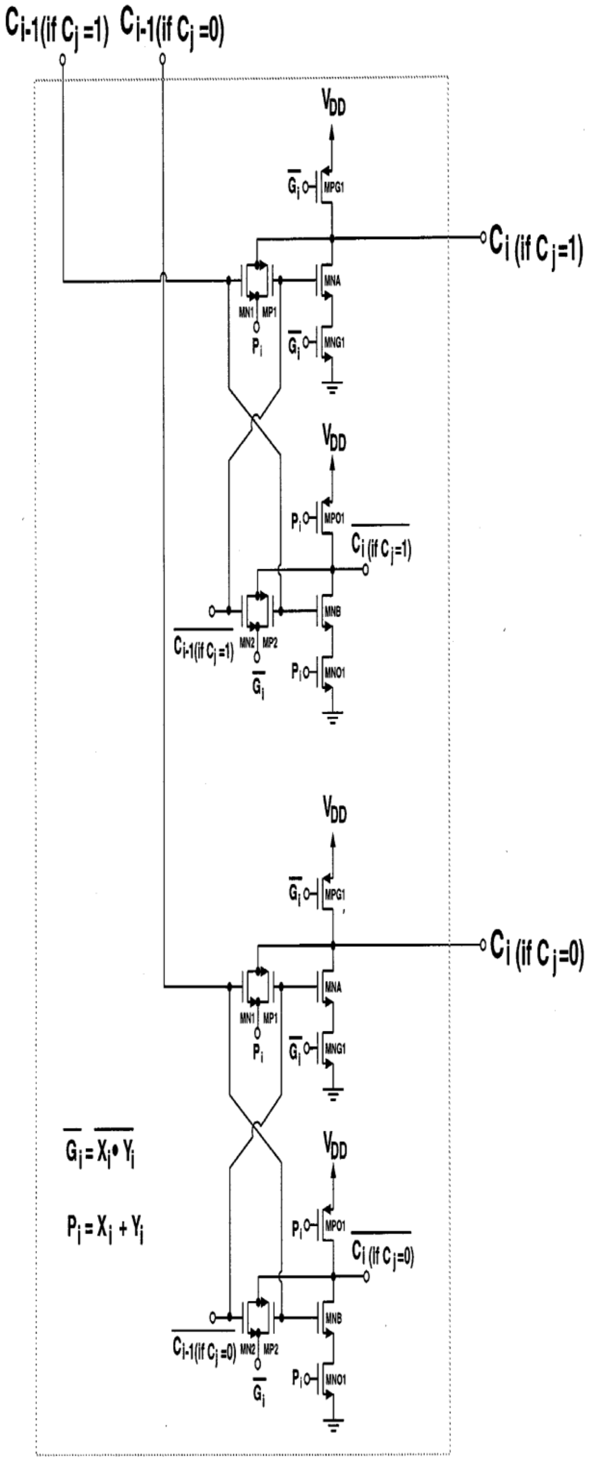

Fig. 3. The 1-bit PTBCS circuit.

Fig. 3 shows the 1-bit pass-transistor-based carry select (PTBCS) . In addition, pass-transistor logic which is 37% faster as compared to the conventional CCS adder without SICNB structure. Fig.5 shows the propagation delay of the 16th bit carry signal (Ci-1) versus the power supply voltage used in the SICNB CCS adder. As shown in the figure, the SICNB CCS adder has a consistent improvement over the conventional CCS adder regardless of the power supply voltage.The power consumption of a 16-bit adder implemented by conventional CCS technique and the SICNB CCS technique. As shown in the fig, using the SICNB CCS technique, the power consumption increases mildly as compared to the adder implemented by the conventional CCS technique. CCS adders have been well known for their advantages in high speed as compared to Manchester adders. The SICNB CCS adder presented in this paper can provide an even higher speed performance as compared to the CCS adder. The applicability of the SICNB CCS adder is discussed here. In this paper, the adder designed is 16-bit. The SICNB CCS adder is also advantageous for implementing adders with more than 16 bits. The critical path of a 32-bit adder implemented by cascading two conventional 16-bit CCS adders involves 16 stages of logic gates.

In contrast, the critical path of a 32-bit adder implemented by cascading two 16-bit SICNB CCS adders involves 12 stages of logic gates, which is 4 stages fewer as compared to the conventional CCS approach. The critical path of a 64-bit adder implemented by cascading four conventional 16-bit CCS adders involves 32 stages of logic gates, which is double as compared to the 32-bit case. On the other hand, the critical path of a 64-bit adder implemented by cascading four SICNB CCS adders, involves 24 stages of logic gates, which is only 50% more as compared to the 32-bit case.

VI. RESULTS: SIMULATION IN S-EDIT

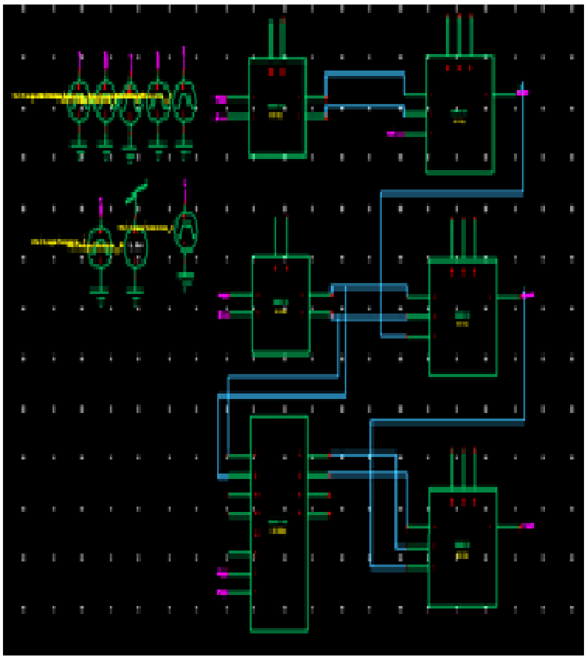

Fig 3 Circuit Diagram of Carry Select adder

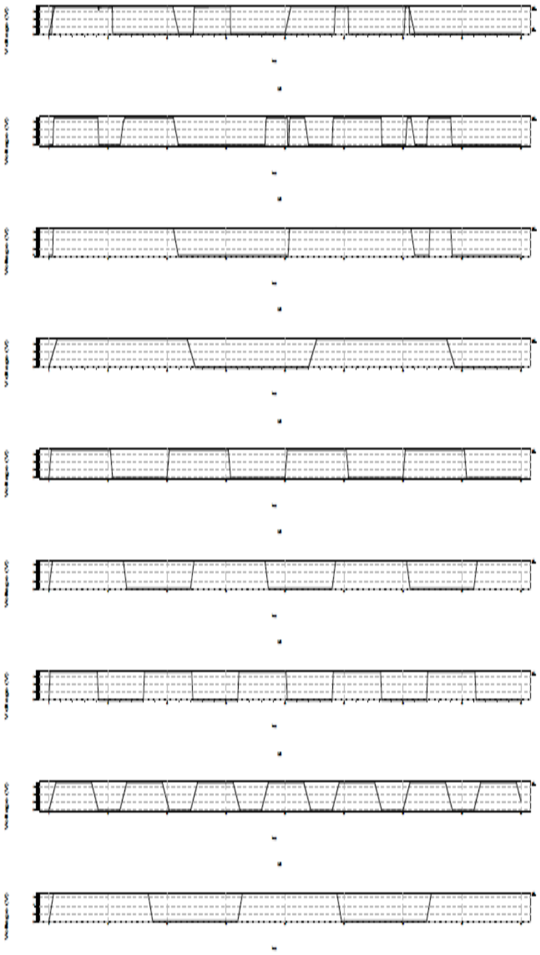

Fig. 5 Waveform of 3 bit Pass Transistor

Circuit was simulated in SPICE Environment. Technology used is 180nm technology with VDD=1.8V as supply voltage. Power is decreased and speed is increased around 37%. .

POWER CALCULATED: 1.63e-06watt

VII. CONCLUSION

In this project, a CCS adder circuit with an SICNB structure for low-voltage VLSI implementation has been described. Owing to the SICNB structure, the new 16-bit SICNB CCS adder provides a 37% faster speed as compared to the conventional CCS adder based on the SPICE results.

VIII. FUTURE SCOPE

From simulation results, we can see that power dissipation is increased, delay is decreased and speed is increased than that of before post layout simulation, then the optimization in the circuit as well as the layout of the proposed carry select adder can be one topic.

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